CLAIMS

What is claimed is:

1. A method, comprising:

decoding a first instruction into a second instruction and a move instruction;

renaming both a first destination register of said second instruction and a second destination register of said move instruction to a physical register; and

retiring either said second instruction or said move instruction responsive to a predicate value.

2. The method of claim 1, wherein said move instruction is responsive to a complement of said predicate value.

3. The method of claim 1, wherein said decoding includes sending a hint to a register renaming circuit.

4. The method of claim 3, wherein said sending includes sending said hint via a trace cache.

5. The method of claim 1, further comprising sequencing said second instruction and said move instruction for out-of-order execution.

6. The method of claim 5, further comprising, when said second instruction executes before said move instruction and said predicate value is true, squashing said move instruction.

7. The method of claim 6, wherein said squashing occurs before said move instruction executes.

8. The method of claim 5, further comprising, when said move instruction executes before said second instruction and said predicate value is false, squashing said second instruction.

9. The method of claim 8, wherein said squashing occurs before said second instruction executes.

10. A processor, comprising:

a decode circuit to decode a first instruction into a second instruction and a move instruction;

a register renaming circuit to map a first destination register of said second instruction to a physical register, and to map a second destination register of said move instruction to said physical register; and

a retirement circuit to update said physical register with a result of either said second instruction or said move instruction responsive to a predicate value.

11. The processor of claim 10, wherein said move instruction is responsive to a complement of said predicate value.

12. The processor of claim 10, wherein said decode circuit sends a hint to said register renaming circuit to permit said map of said first destination register and said second destination register to said physical register.

13. The processor of claim 12, wherein said hint is sent via a trace cache.

14. The processor of claim 10, further comprising a sequencer to permit out-of-order execution of said second instruction and said move instruction.

15. The processor of claim 14, wherein said retirement circuit may squash said move instruction when said second instruction executes before said move instruction and said predicate value is true.

16. The processor of claim 14, wherein said retirement circuit may squash said second instruction when said move instruction executes before said second instruction and said predicate value is false.

17. The processor of claim 14, further comprising execution units to execute said second instruction and said move instruction in parallel.

18. A processor, comprising:

means for decoding a first instruction into a second instruction and a move instruction;

means for renaming both a first destination register of said second instruction and a second destination register of said move instruction to a physical register; and

means for retiring either said second instruction or said move instruction responsive to a predicate value.

19. The processor of claim 18, wherein said move instruction is responsive to a complement of said predicate value.

20. The processor of claim 18, wherein said means for decoding includes means for sending a hint to a register renaming circuit.

21. The processor of claim 18, further comprising means for sequencing said second instruction and said move instruction for out-of-order execution.

22. The processor of claim 21, further comprising means for squashing said move instruction when said second instruction executes before said move instruction and said predicate value is true.

23. The processor of claim 21, further comprising means for squashing said second instruction when said move instruction executes before said second instruction and said predicate value is false.

24. A system, comprising:

a processor, including a decode circuit to decode a first instruction into a second instruction and a move instruction, a register renaming circuit to map a first destination register of said second instruction to a physical register, and to map a second destination register of said move instruction to said physical register, and a retirement circuit to update said physical register with a result of either said second instruction or said move instruction responsive to a predicate value;

a bus to couple said processor to input/output devices; and

a communications device coupled to said bus.

25. The system of claim 24, wherein said move instruction is responsive to a complement of said predicate value.

26. The system of claim 24, wherein said decode circuit sends a hint to said register renaming circuit to permit said map of said first destination register and said second destination register to said physical register.

27. The system of claim 24, further comprising a sequencer to permit out-of-order execution of said second instruction and said move instruction.

28. The system of claim 27, wherein said retirement circuit may squash said move instruction when said second instruction executes before said move instruction and said predicate value is true.

29. The system of claim 27, wherein said retirement circuit may squash said second instruction when said move instruction executes before said second instruction and said predicate value is false.